Options for PMT Electronics at the Hyper-K Far Detector

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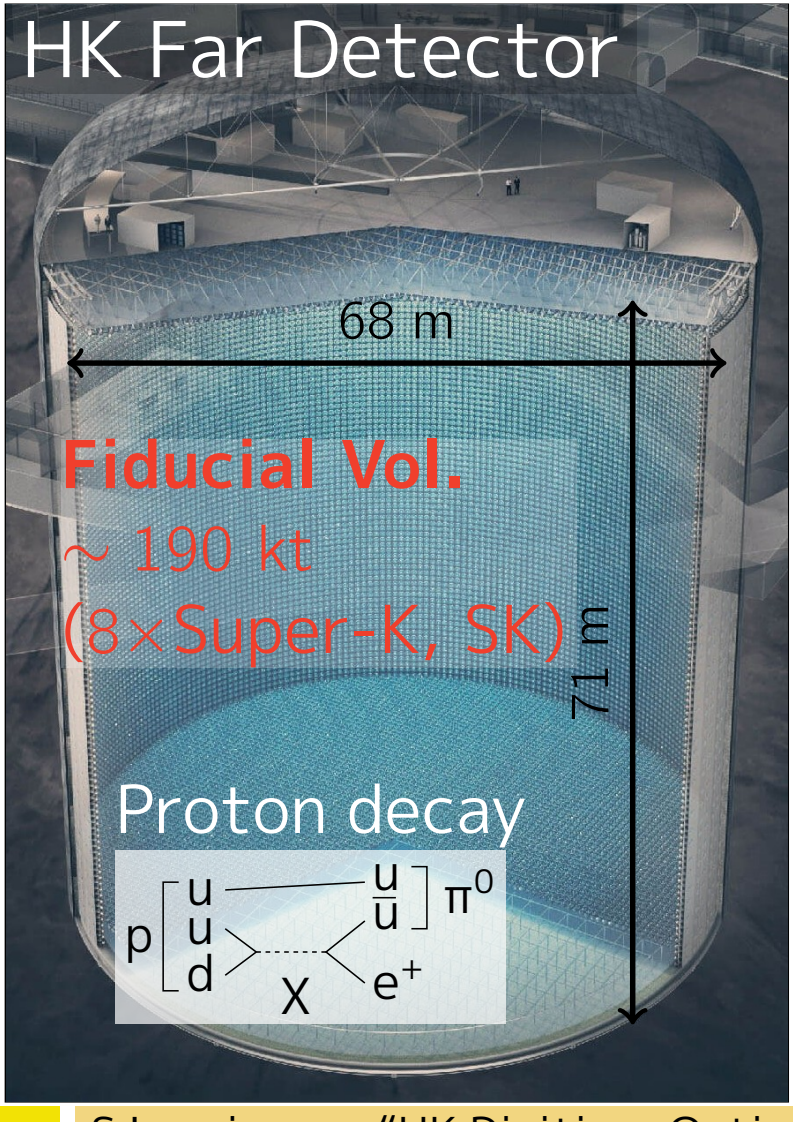
for Hyper-Kamiokande Collaboration

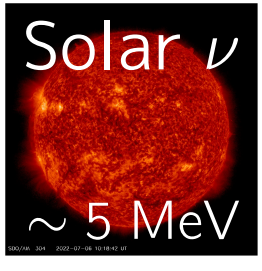
NuFACT 2022 (Utah), 2 Aug. 2022

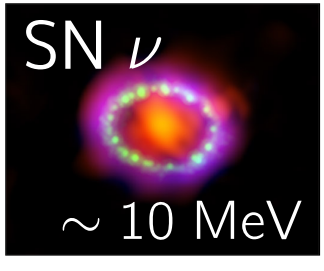
Hyper-Kamiokande Project (HK)

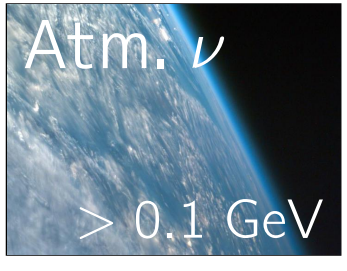
⇒ 3rd gen. Water Cherenkov Detector



+ J-PARC ν beam complex







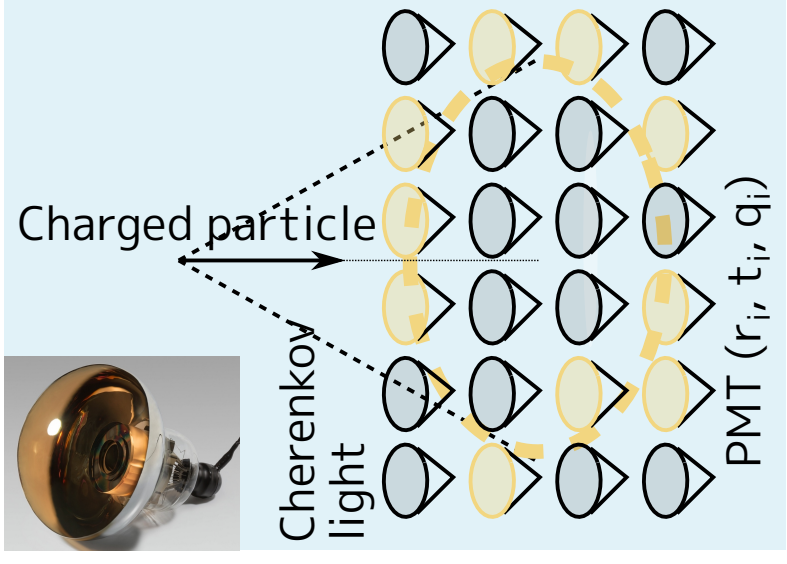
⇒ Energy: 1 MeV ~ 1 TeV

Operation: 2027 ~

Credits: [Sun] NASA/SDO and the AIA, EVE, and HMI science teams.,
[SN1987] NASA Chandra X-ray observatory,
[Earth] NASA Glenn Research Center.

Detector Principle and PMT

- Cherenkov Ring Imaging Detector
  - $\Rightarrow$ Ring shape with 5-dimension $(\boldsymbol{r}, t, q)$



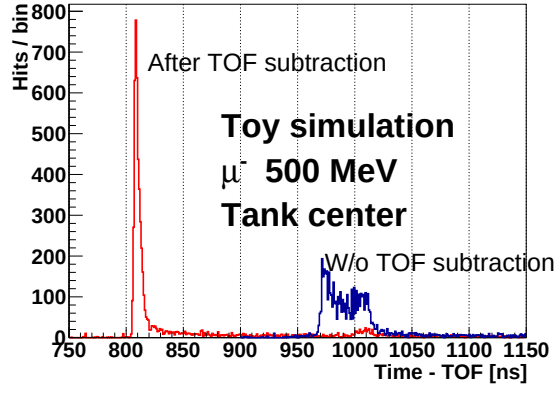
Position $\boldsymbol{r}_i$

Timing t_i

Charge q_i

Interaction vertex

Finding point giving sharpest peak in t-dist.

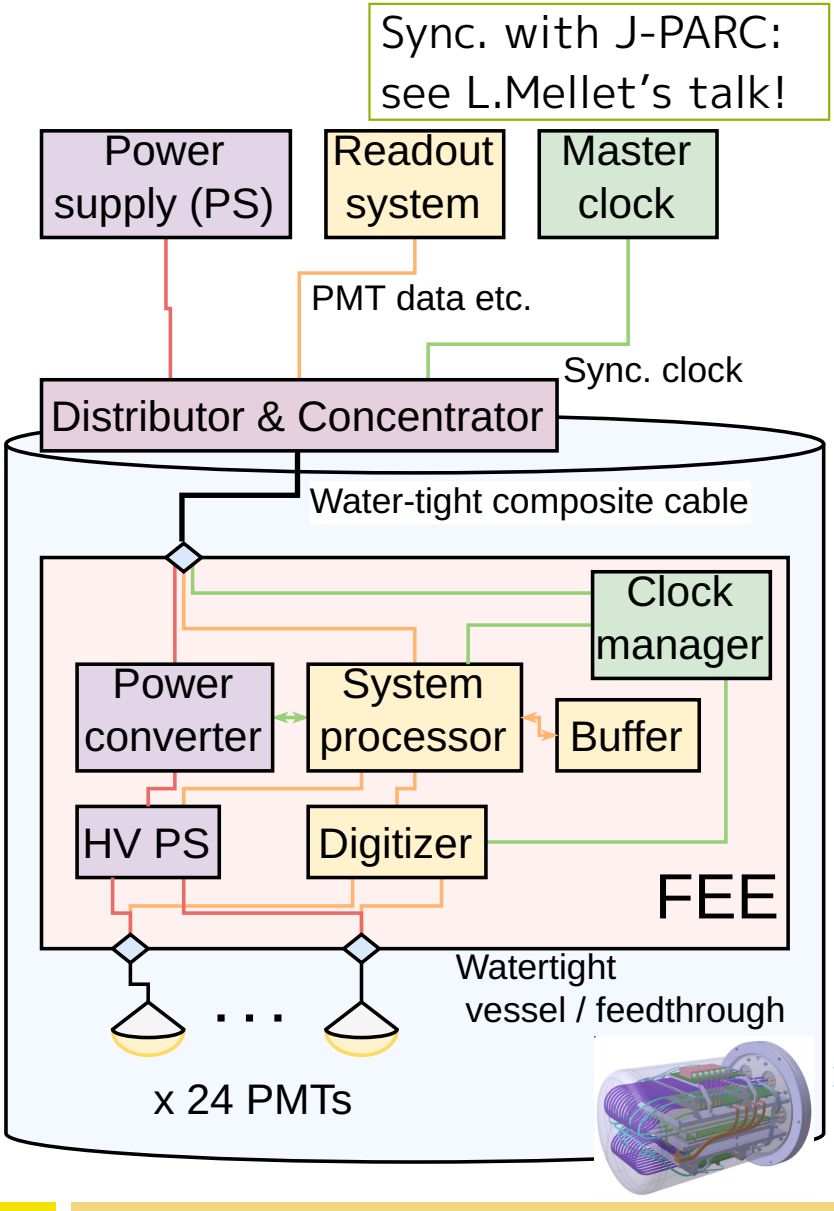


Correction

Energy

- **20-inch PMT: improved from SK $\rightarrow$ twice better**
  Timing res., quantum eff. $\times$ collection eff., charge res.

Electronics of Far Detector



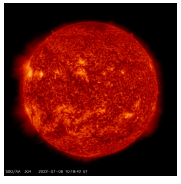
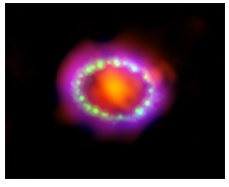
- Photosensors:
  - Inner detector (ID):
    ~ **20,000 20-inch PMTs**
    + ~ 1,000 mPMTs
  - Outer detector (OD):
    ~ 8,000 3-inch PMTs
- 1,000 underwater vessels
  - Front-End Electronics (FEE) and HV for ID+OD PMT

  ⇒ Reliability: critical

⇒ Final design in Nov. 2023

Requirement to Digitizer (1–50 MeV)

Low energy: 1–50 MeV

- Num. of PMT pulse $\sim$ 10/MeV

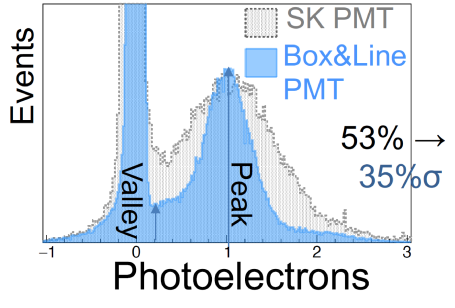
$\Rightarrow$ Single photon detection

- Nearby SN:
  $\sim$ 180 M events in 10 s

$\Rightarrow$ PMT signal rate $\sim$ 1 MHz

PMT response

- Timing res. $\sim$ 1.1 ns
- Charge res. $\sim$ 31 %
- Q dynamic range
  $\sim$ 1–1000 pe

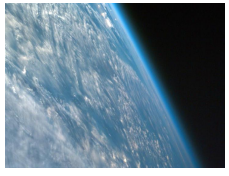


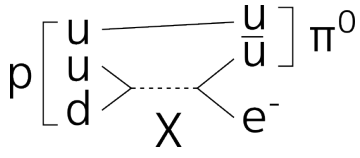
Requirements to digitizer

- Low noise & low threshold
- Maximizing PMT performance
  - Timing resolution

Requirement to Digitizer (> 100 MeV)

High energy ⇒ > 100 MeV





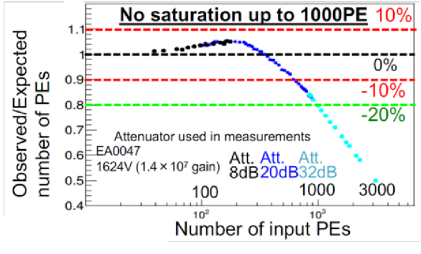
⇒ Dynamic range of ~ 1000 p.e.

- Decay-electron from muon
  - ID of invisible μ,π

⇒ Lifetime ~ 2.2 μs

PMT response

- Timing res. ~ 1.1 ns
- Charge res. ~ 31 %
- Q dynamic range ~ 1–1000 pe



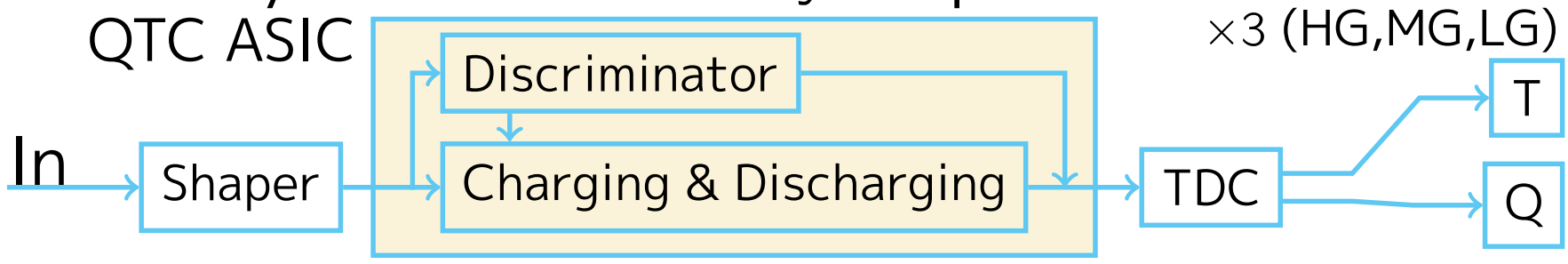
Requirements to digitizer

- Maximizing PMT performance
  - Charge res. & dynamic range & linearity
- Deadtime < 1 μs

Three Options for HK Digitizer

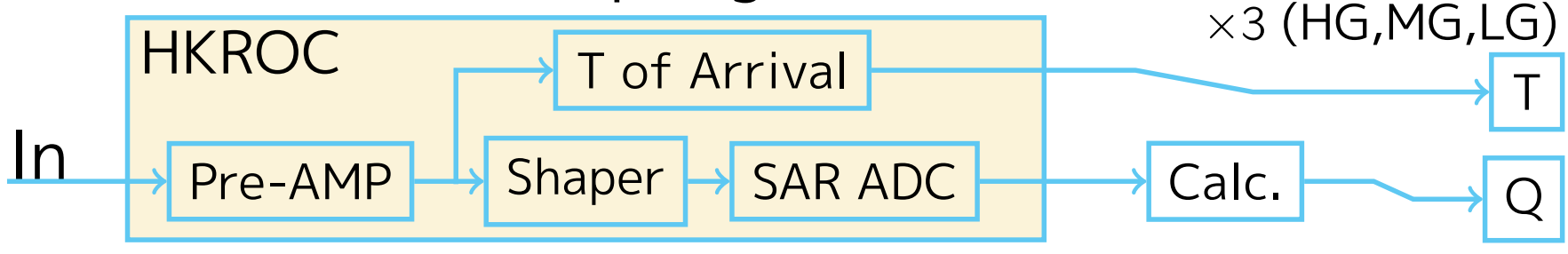
QTC+TDC

Reliability based on > 10 yr experience in SK



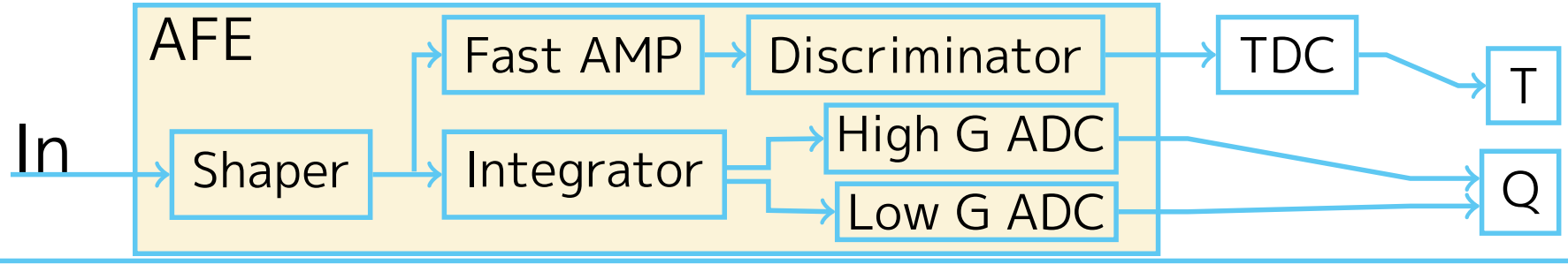
HKROC

New waveform-sampling ASIC



Discrete

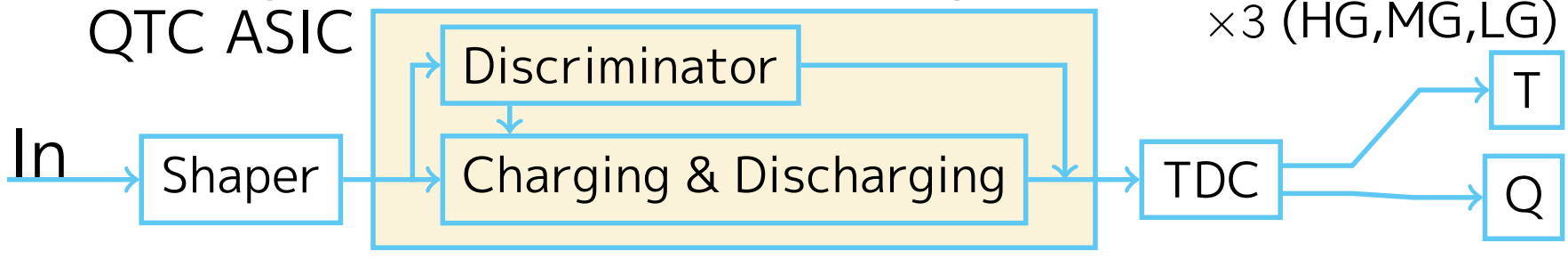
Tunability with discrete components

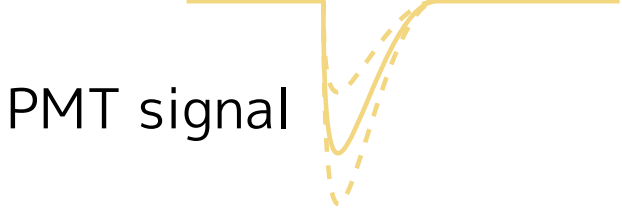


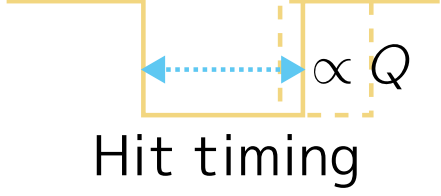
Option1: QTC+TDC

QTC+TDC

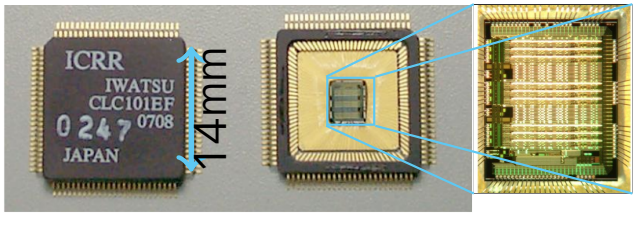
Reliability based on > 10 yr experience in SK



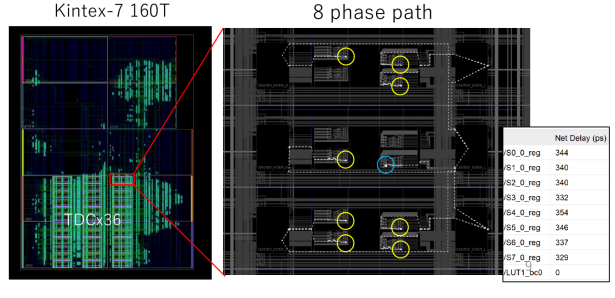




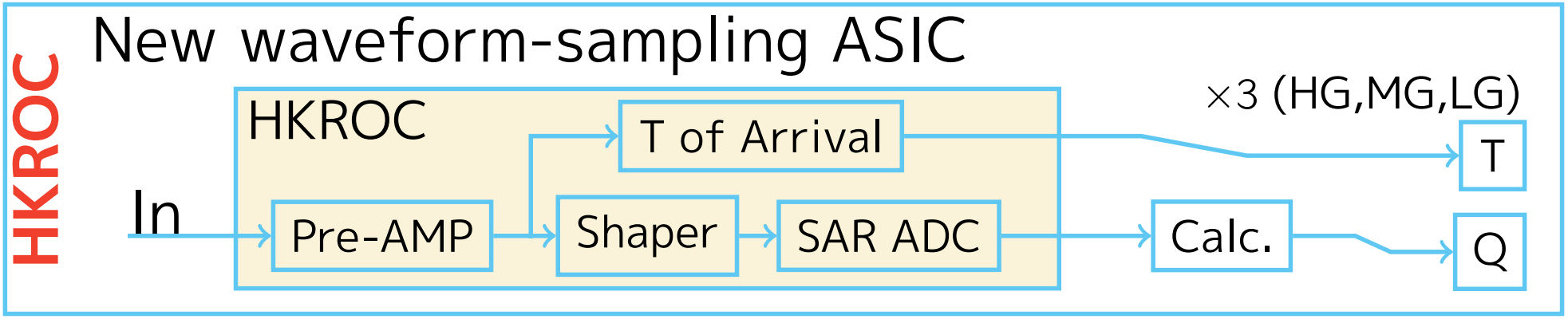
- Charge-to-Time Conv. (QTC)
  - Custom ASIC for SK
  - Established reliability by > 10 yr operation in SK
- Time-to-Digital Conv. (TDC)
  - Newly developed in FPGA for HK

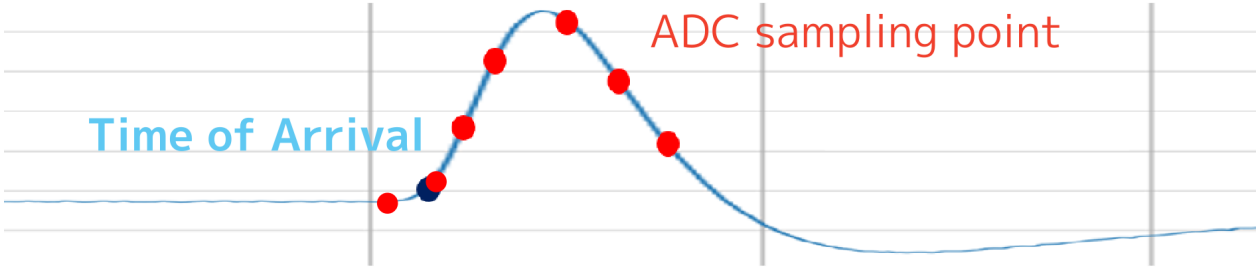


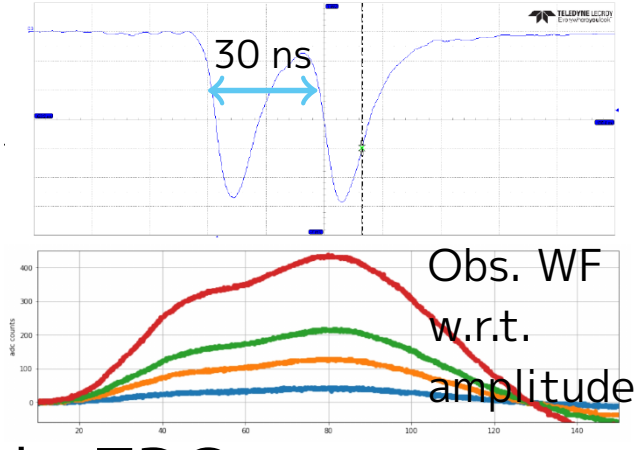
NIMA610:710-717,2009



Option2: HKROC







- Waveform sampling ASIC
  - Based on HGCROC (CMS HGCalorimeter)
  - Sampling ADC + Time of Arrival via TDC
    - 40 MSPS, configurable number of sampling points

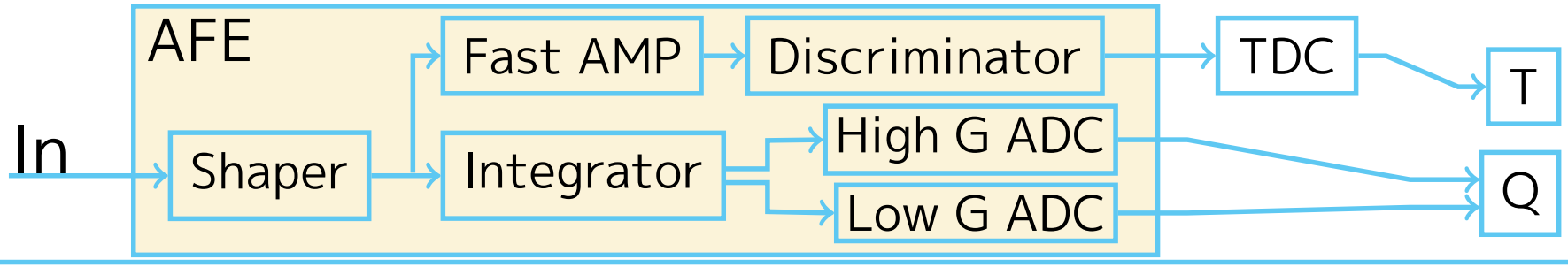
⇒ Signal separation: $\Delta t > 30$ ns

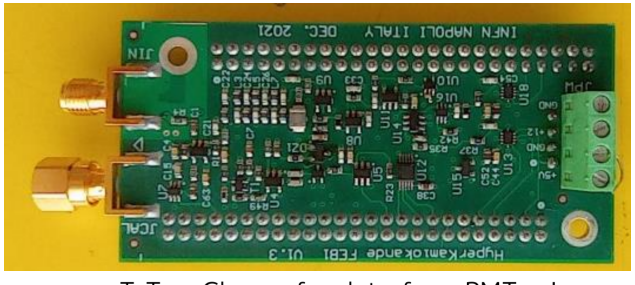
  - Reduced deadtime ⇒ decay-e and nearby SN

Option3: Discrete Type

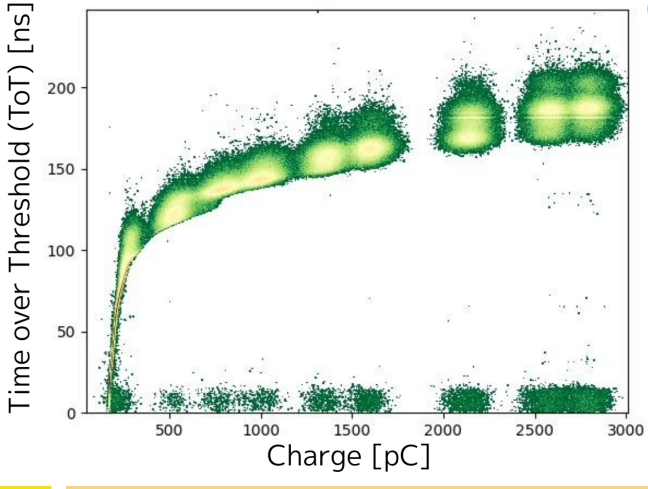
Discrete

Tunability with discrete components





ToT vs Charge for data from PMT + Laser



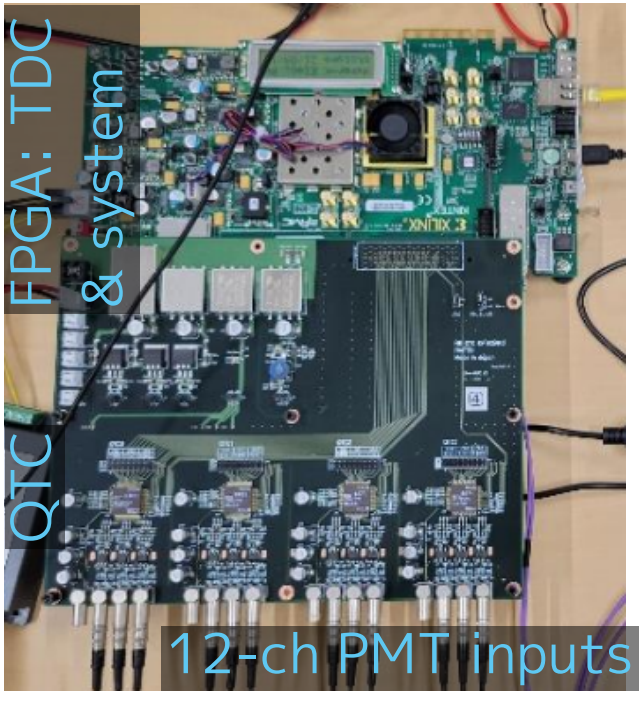
- Highly tunable / flexible circuit with discrete parts
  - Components: op-amp, ADC
- Time over Threshold (ToT)
  - Complementary information with integrated Q by ADC

⇒ May help to separate noise / pre-pulse / late-pulse

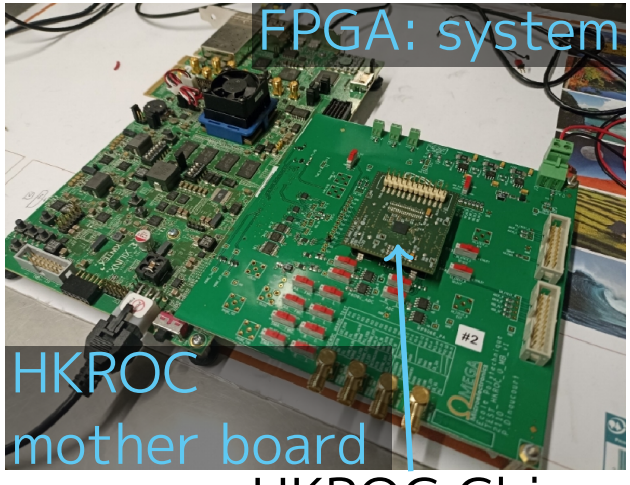
R&D Status: Full Functional Model 11/15

Prototypes of digitizers for performance evaluation

QTC+TDC



HKROC



HKROC Chip

Discrete

24 ch analog frontends

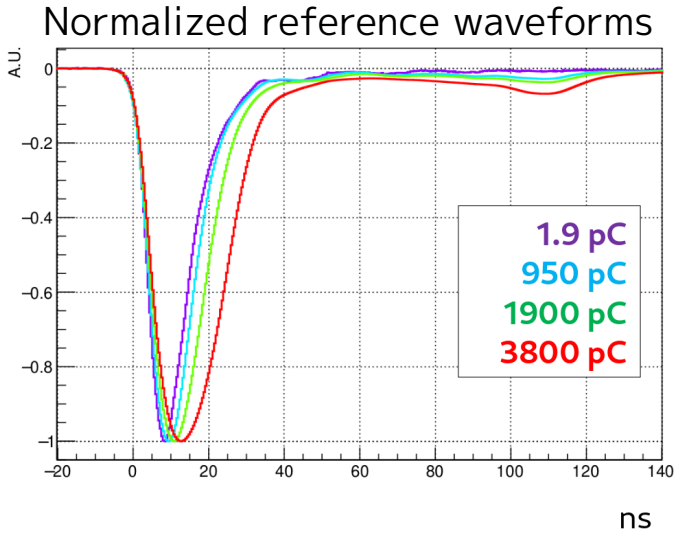
⇒ Next revision: single board with all functions

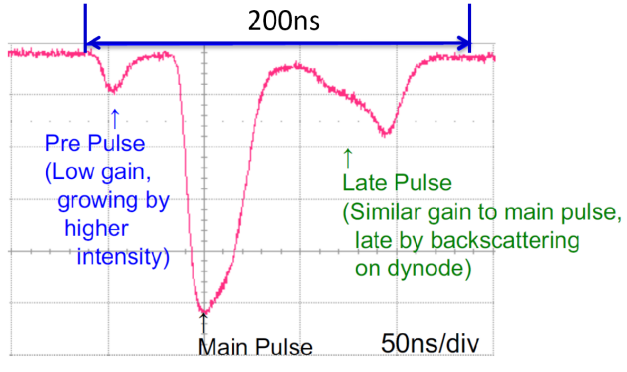
- Integration with OD digitizers, size optimization etc.

Evaluation of Digitizers

1. Basic performance with FG
   - Deterministic signal
     - Stable noise, and configurable pulse timing and amplitude
2. Confirmation with PMT
   - AC coupled system
   - Stochastic signal
     - Noise and pre-/late-/after-pulse
     - Termination and reflections
     - Handling of baseline fluctuation

⇒ Important cross validation

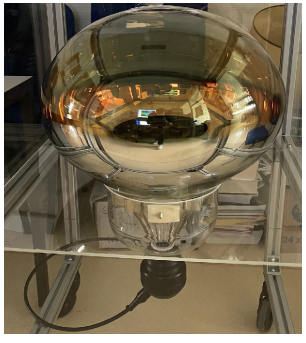


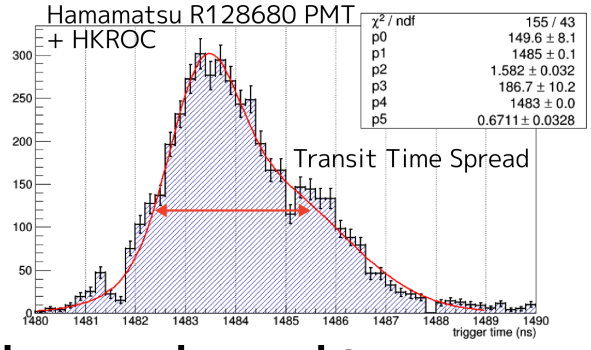


3. Response to environment: ESD, temperature
4. Circuit simulation: power, heat, reflection etc.

Evaluation of Digitizers (example)

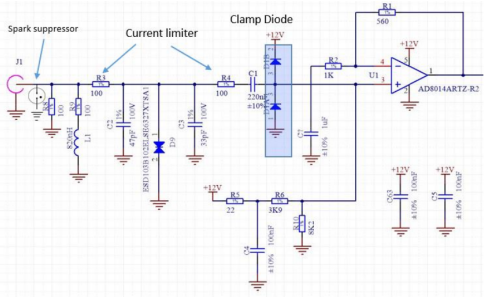
Readout from 20" PMT

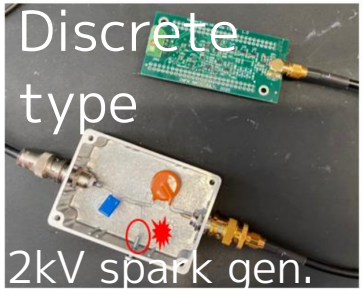




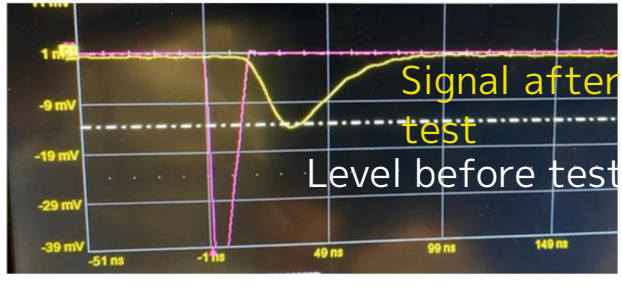
PMT characters are reproduced: charge res., timing res., linearity, etc.

Protection circuit



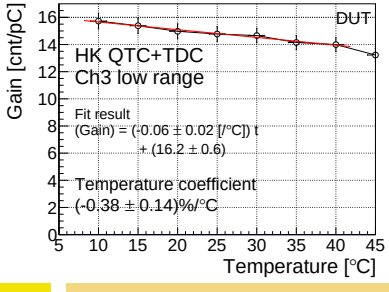


Signal after 1000 discharges

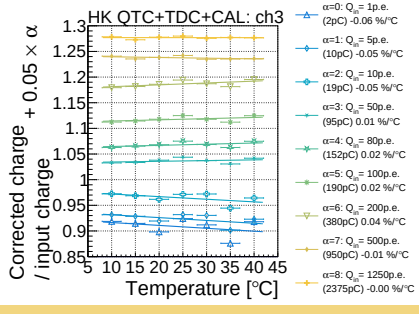


No degradation after ESD test

Temperature coefficient



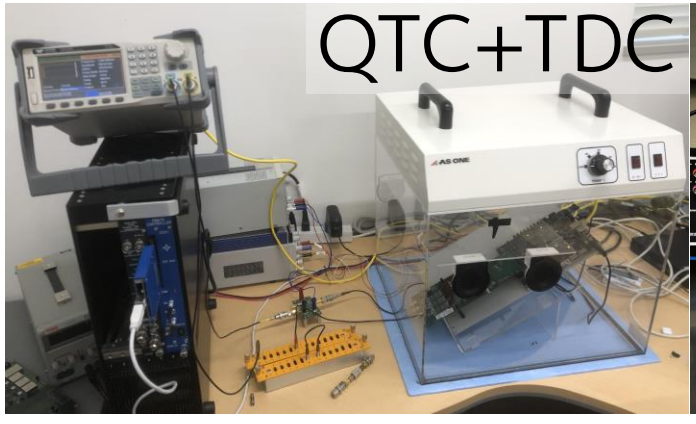
Calibrator: variable amplitude

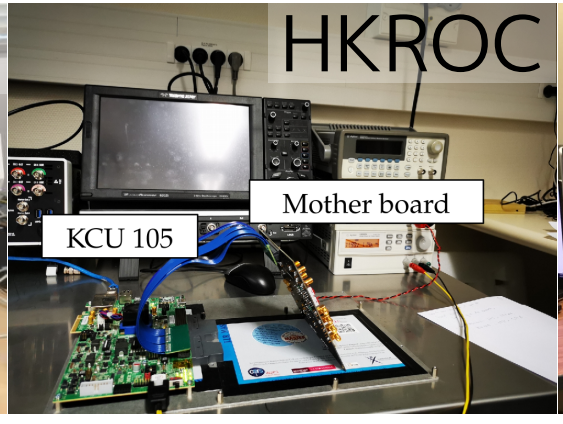


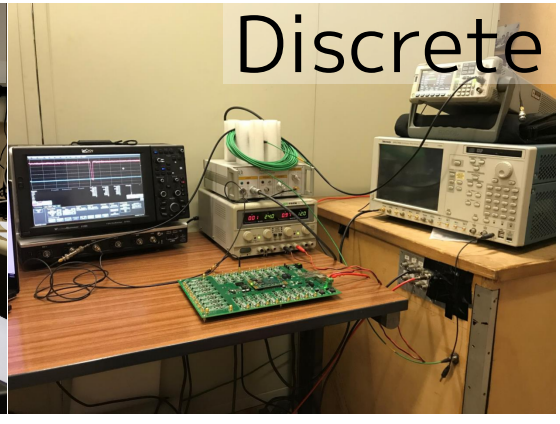
Many other tests (all options): reflection, cross-talk, rate capability, FIT calc. etc.

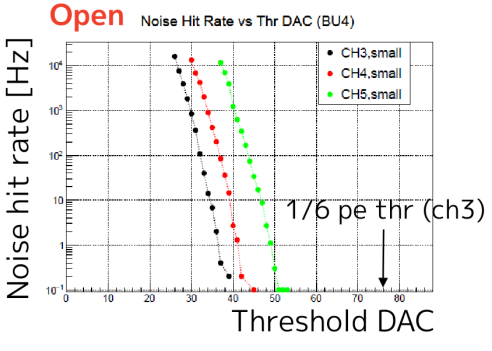
Status of Measurements

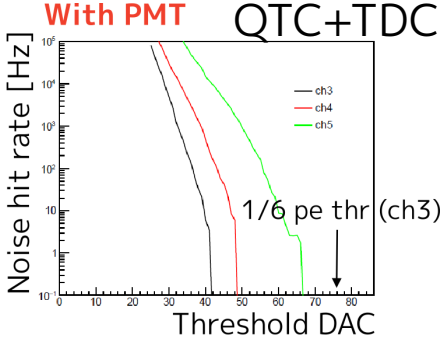
Measuring performance in parallel

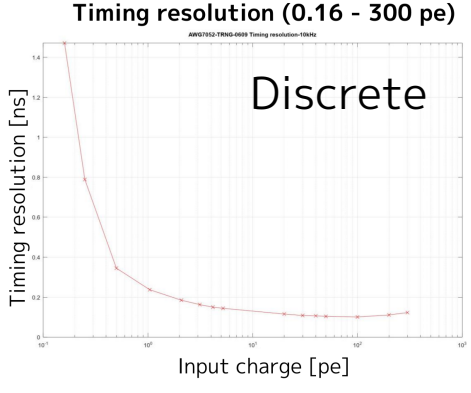


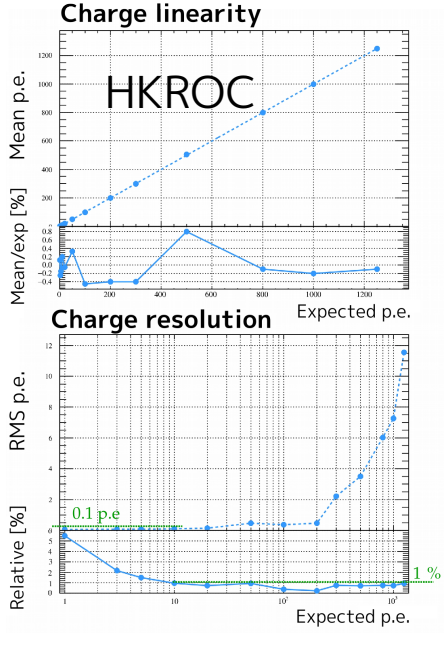












⇒ Results of measurements are being reviewed in collaboration

- Basic requirements: satisfied

Summary and Prospect

- Hyper-Kamiokande: water Cherenkov detector
  - FV ~ 190 kt, 20,000 of 20" PMTs + 1,000 mPMTs
  - Planning to start operation in 2027
- Three options of digitizer for 20" PMTs
  - **QTC ASIC + TDC**: experience over 10 yr in SK
  - **HKROC**: new waveform-sampling ASIC
  - **Discrete type**: tunability & flexibility
- Schedule
  - Collaboration review is ongoing to select one option

⇒ Starting R&D of integrated design of ID and OD PMTs

⇒ 2023 May. → 2023 Nov.

Start of **system-test in vessel and underwater**

Freezing design of FEE

Starting designing of mass-production model

Appendix

Requirements to Digitizer

Basic performance required to digitizers

Timing resolution	0.3 ns (1 pe) 0.2 ns (>5 pe)
Charge resolution	0.1 pe (<10 pe) 1 % (>10 pe)
Charge dynamic range	1–1250 pe
Charge linearity	≤ 1 %
Discri. threshold	$<1/6$ pe

Practical characters

Dead-time, hit rate, failure rate, cross talk, SN ratio, temperature coefficient, ESD tolerance, power consumption, etc.

QTC+TDC: QTC detail

QTC ASIC

* FIT=# of failures in 10^9 hours

- developed and used for SK since 2008
  - ✓ no failure in ID = low failure rate confirmed (FIT<1.68)
- 3 range channels cover dynamic range ~1250pe
  - ✓ triggers of 3 range discriminators are ORed.
- production line 0.35 μ m CMOS is still active
  - ✓ We propose to use QTC with updated peripherals (TDC, input circuit, etc) for HK.

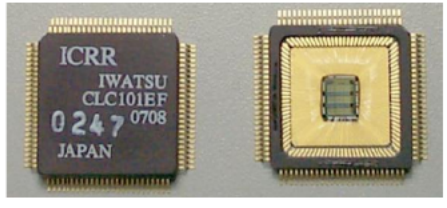


Diagram for 1PMT channel

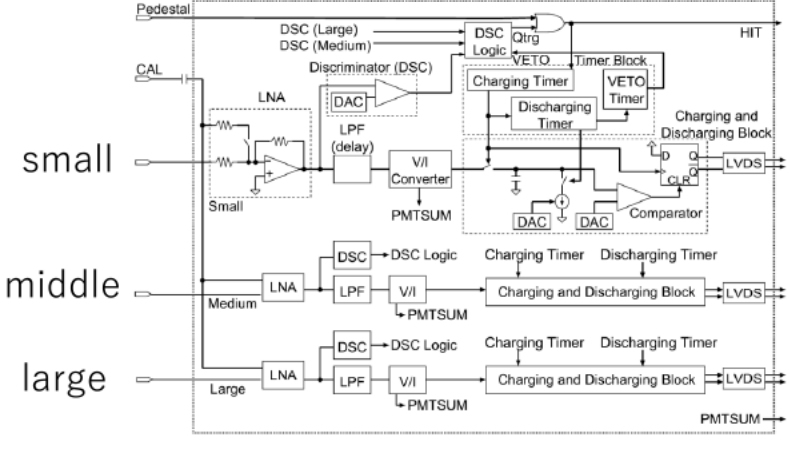


Table 1: QTC specification.

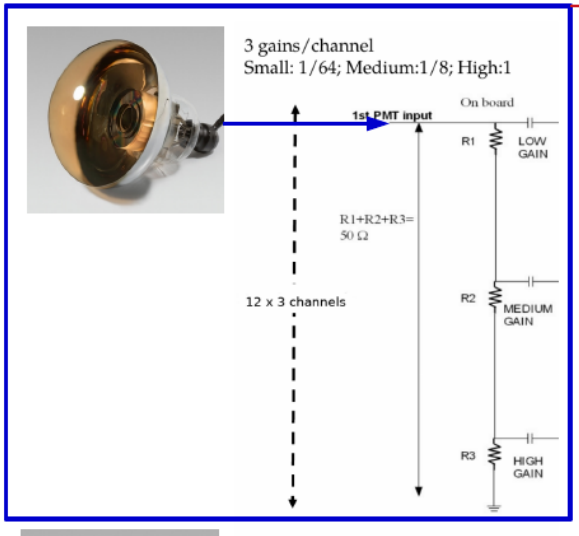
Item	
Number of input per chip	3 PMT channels
Trigger	self trigger with constant threshold
Threshold	-0.3 ~ -14 mV
Input voltage	> -3 V
Dynamic range	0.25 ~2,500 pC with 3 ranges
Charge gate	50~500 nsec (6 bit)
Processing time	316~766 nsec (6 bit)
Charge Resolution	~0.15 pC (< 50 pC)
Charge (Non-)Linearity	< ±1 %
Timing Resolution	0.2 ns (-3 mV)
Power dissipation	260 mW/chip
Process	0.35 μm CMOS process
Package	100 pin CQFP package

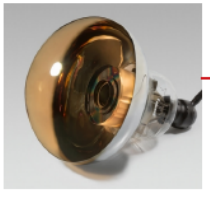
6

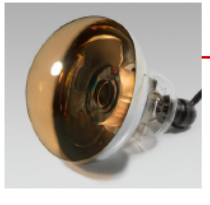
HKROC: block diagram

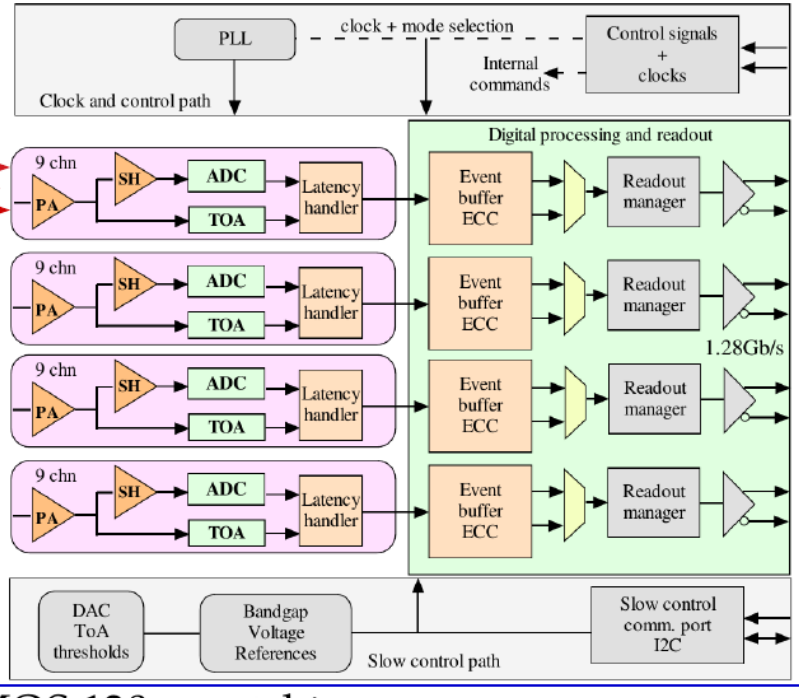
The HKROC digitizer

- Based on HKROC chip : 12 PMTs ↔ 36 channels (high,medium,low gain)









- TSMC CMOS 130nm etching.
- Dynamic range from 0 – 2500 pC : 3 gains / channel.
- 4 readout / ASIC @1.28 Gb/s : 1 readout ↔ 3 PMTs.
- If 1 PMT trigger : read all 3 PMTs of 1 readout.

Discrete: block diagram

FE Discrete Digitizer Board: FE circuit design

- The circuit is based on discrete ICs
  - Developed by NA group
- PMT input signal feeds 2 paths:
  - Integrator for CHARGE measurement
  - Fast Discriminator for hit TIMING
- Final design uses Baseline Restore Enable technique